Improved Stress Distribution in Railway Traction Converters Using New High Power Half-Bridge Modules

Michel Piton, Emmanuel Batista, Vincent Escrouzailles
Alstom, Traction system engineering, Rue du Docteur Guinier 65601 Séméac France

Abstract

New High Power Half-Bridge Modules have recently been introduced in railway traction converters. They are designed to minimize stray inductance and get full benefits of modern fast switching power Si IGBT and SiC MOSFET. These new standard modules available in different voltage classes offer to the user advantage of scalability and improved power ratio.
Electrical and thermo-mechanical stress distribution in the converter is also important as it can impact strongly reliability and lifetime which are key requirements for railway traction applications.
Thanks to advanced multi-domain simulations based on Reduced Order Model (ROM) technique and measurements, non uniformity of current and temperature stress between chips is analyzed in case of a realistic mission profile. Electrical and thermal stress distribution is improved compared to state-of-the art converters. A very good current distribution between paralleled chips is reported (# 3 %), a reduction of temperature difference between paralleled chips (typically reduced by half) is estimated with a direct impact on lifetime.

1 Introduction

Standard high power IGBT modules in 190x140 mm package introduced in the late 90's are today mainstream for railway traction converter design covering the whole range of rolling stocks in terms of current (up to 3600 A) and voltage (1700 V to 6500 V).
Nevertheless, these packages are reaching their limits especially in terms of stray inductance to adapt to last generations of power semi-conductors with fast switching features (Si IGBT and SiC MOSFET).
New High Power Half-Bridge Modules have recently been introduced to overcome these limitations and take full benefit of last generation of semiconductor power devices. A common requirement specification for railway traction applications was released based on discussions between converter manufacturers and railway operators in the frame of Shift2Rail European program [1].
These new modules offer improved power density (Figure 1) and lower losses leading to improved converter compacity. For a typical inverter leg function using 3300 V Si IGBT, a reduction of 25 % of module area reduction is achieved.

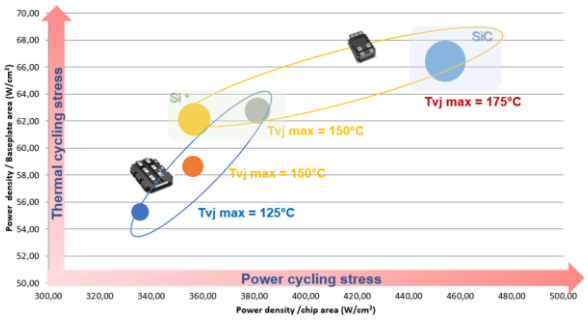


Figure 1 Evolution of power density of semiconductor power devices used in railway traction converters.

In addition to improve converter performances, high reliability over the whole lifetime (typically 30 years) is expected by railway operators. Reliability and lifetime are therefore key requirement for railway traction application.
This paper analyzes the benefits of New High Power Half-Bridge Modules brought in terms of stress distribution in the converter resulting directly in improved reliability and lifetime.

2 Electrical and thermal stress distribution in railway traction converters

2.1 Origin and impact of stress distribution in high power semiconductor modules

High power IGBT multichip modules in railway traction converters are (sub)systems containing a large number of paralleled dies to meet the need of high current capability (typically a few 1000 A). Keeping current unbalance between paralleled chips at an acceptable level has always been a challenge especially in high power field and during transient phases. Current unbalance can be generated by internal construction of the module but also induced by converter design itself. These unbalances are directly affecting robustness of converter but are also inducing chip temperature differences leading in turn to lifetime differences. These effects cannot be neglected as they may induce predominant effects in terms of reliability and lifetime.

As a consequence, stress distribution within a converter must be carefully assessed during design phase in order to be minimized. In this paper, current and temperature

stress distribution in a converter using New High Power Half-Bridge Modules is analysed and compared to state-of-the-art railway converters.

2.2 Quantifying stress distribution by multi-domain simulation

Improved computational capability offers possibilities to develop advanced multi-domain simulation approach. In order to predict the switching behavior due to electromagnetic parasitic elements, electrical equivalent circuits based on Reduced Order Model technique (ROM) can be built to represent accurately the 3D design of the power module into circuit simulator [5]. Figure 2 represents an example of electrical circuit linking ROMs - for a module (in green) and the power connections (in orange) - to IGBT models (in blue). Thanks to this approach and with a dedicated control law (in yellow), the current sharing between chips can be predicted in a double pulse test configuration.
This can be used to have an insight view of current and temperature stress distribution inside the module integrated in a converter and to optimize converter design.

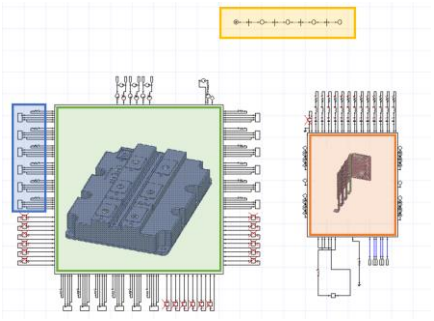


Figure 2 Multi-domain simulation environment linking 3D models to active and passive electrical components.

A thermal 3D model has been built to estimate the junction temperature of each chip depending on their position in the module. In this study, the thermal behavior has been used as a ROM and has been linked to the electrical ROM described previously. The complete workflow is represented on figure 3 where:

1) the electrical ROM takes into account the parasitic impedance of the design and chip electrical characteristic depending on temperature i.e. On state voltage and gate threshold voltage.
2) the thermal ROM takes into account the chip electrical losses as inputs and calculate the junction temperature at chip level as outputs

The main advantage of this workflow is to be able to link recursively the chip junction temperatures as inputs for Von(T) and Vgth(T). In this way, those electrical characteristics can evolve at each time step (dt) during the complete route profile depending on the temperature elevation.

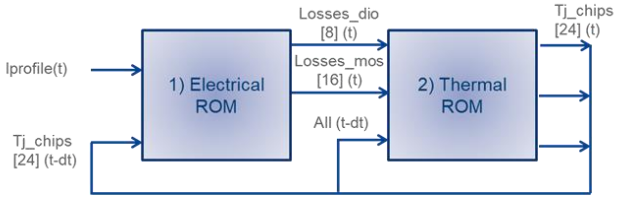


Figure 3 Multi-domain simulation workflow coupling electrical and thermal ROM on the complete route profile current.

3 Comparison of switching behavior between the two switches of Half-Bridge Module

With a standard single switch module topology, copper connections and specifically phase copper bar connecting the two switches externally induce differences between top and bottom IGBT during turn-on and turn-off. In addition, it is generally not possible to keep a “strip line” converter layout due to integration constraints. Figure 4 illustrates the influence of the busbar and phase copper bar in terms of current repartition.

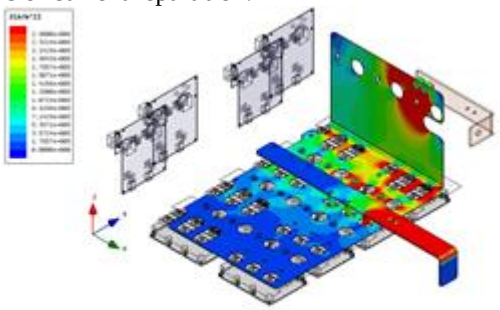


Figure 4 3D current density cartography for an inverter leg copper bar and busbar.

In the case of New High Power Half-Bridge Module, phase connection length is minimized as it is done inside the module and the “strip line” layout can be kept in the converter design [8],[9].

	Converter Leg Stray Inductance (DC value)
Single switch	**80 nH**
New Half bridge module	**30 nH**

Figure 5 Comparison of simulated stray inductance (DC value) in case of single switch and half bridge

As shown in figure 6, similar switching behavior is observed between top and bottom switches of New High Power Half-Bridge Module.

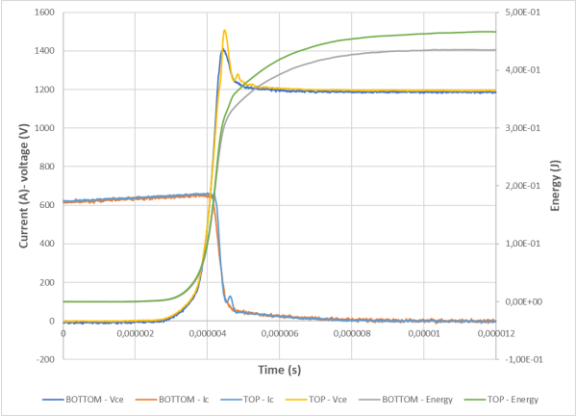
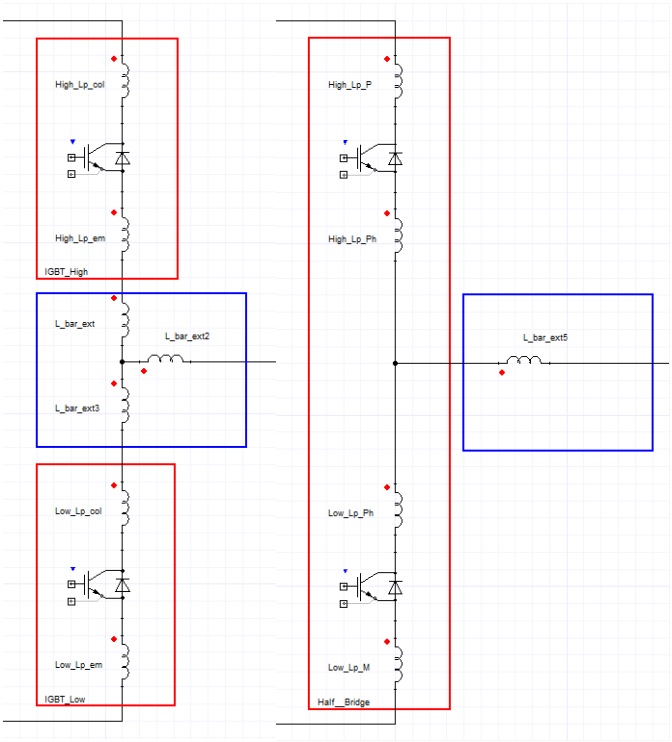


Figure 6 Comparison of switching behavior between top and bottom switch of New High Power Half-Bridge Module.

Due to symmetrical design at module and connection (busbar) level, the differences between switches are now reduced. It is interesting to note that with the new design of half-bridge module, the converter external phase copper bar (in blue in the figure 7b) is no longer part of the power loop and no longer influences the differences between high and low switches.
As described in the figure 7a, classical single switch inverter leg had a part of the phase copper bar included in the loop impedance which influences the switching behavior of both single switches (in red).



a) b)

Figure 7 Parasitic impedance distribution differences between classical single switch inverter leg a) and Half-bridge module b).

Simulation also makes possible to predict the behavior of the current at chip level while it is not accessible easily by measurement. Indeed, the current distribution can be degraded due to module design and, as shown on figure 8 for a single switch, have impact on the static current – 20 % of difference between the lowest and the highest chip current is observed – and introducing delay on the dynamic phase – around 100ns delay between the first and the last chip switching.

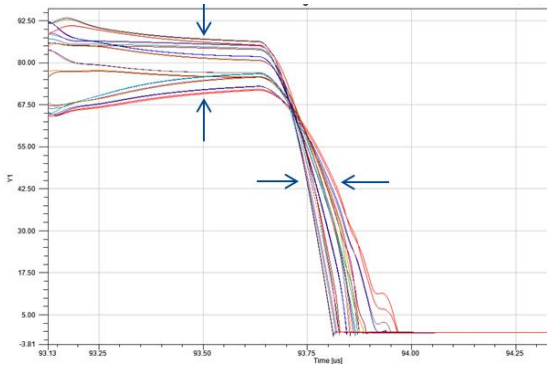


Figure 8 Simulation of current distribution during turn-off between IGBT chips for a single switch

With the same simulation methodology applied to New High Power Half-Bridge module 3D design, the current distribution at chip level is given on figure 9. The simulation confirms the good current distribution with less than 2 % difference and with a switching delay lower than 20ns.

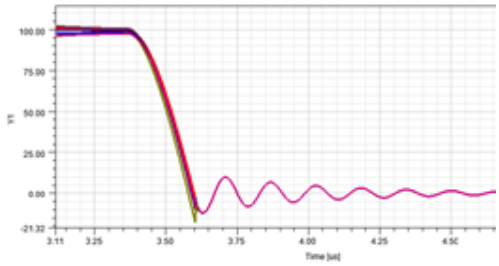


Figure 9 Simulation of current distribution during turn-off between IGBT chips for a New High Power Half-Bridge

New High Power Half-Bridge Module offers the possibility of easier strip line converter design and shows a smaller gap between the lowest and highest chip current for both static and dynamic phases.
Paralleling of chips inside a module is improved, however paralleling several New High Power Half-Bridge Modules which is necessary to reach high current required for high power application should not be neglected. It is challenging to parallel several New High Power Half-Bridge Modules especially regarding interface with gate driver. Within Shift2Rail program, a reference test set-up for paralleling has been defined [2].

4 Impact of temperature distribution on converter lifetime

Current unbalance discussed in §3 results in chip temperature difference that can be added to temperature differences induced by cooling system [4]. Temperature difference between chips is important as the hottest chip will determine the reliability and lifetime of the whole converter [10]. Impact of most loaded chip on lifetime in power / thermal cycling must be analyzed.

By simulation, the current unbalance at chip level can be computed on a complete route profile and coupled to a thermal model in order to estimate the chip junction temperatures. An example with a single switch composed of 24 IGBT chips is illustrated for a 4000s typical metro route profile on figures 10 and 11, respectively the current and the junction temperature distribution between chips. This simulation shows a temperature difference between the coolest and the hottest chip up to 10 K.

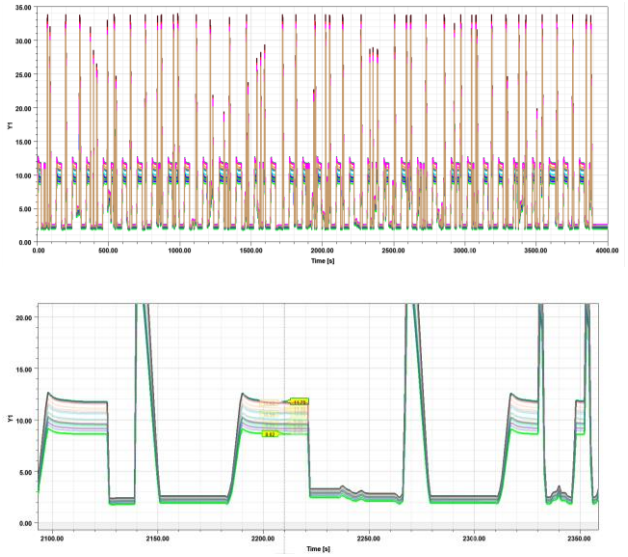


Figure 10 Single switch chip current unbalance simulation on a complete route profile.

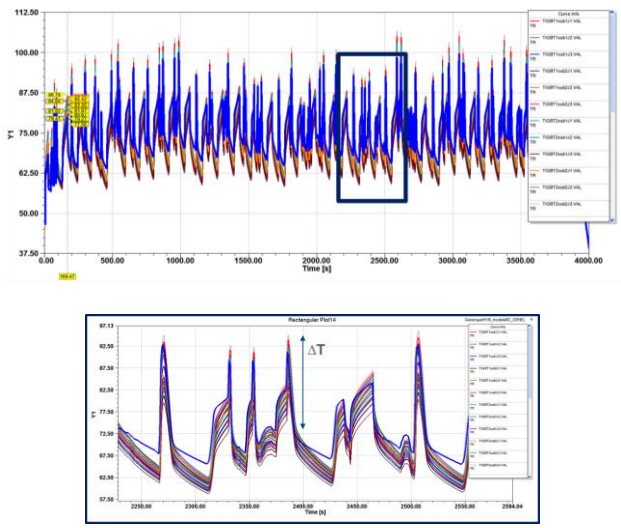


Figure 11 Single switch chip junction temperatures unbalance simulation on a complete route profile.

Based on these results, the lifetime is calculated using Rainflow ΔT counting methodology [6]. The histogram of figure 12 represents the lifetime gap from mean value in % for each 24 IGBT chips. For the hottest chip identified, a lifetime reduction of 60% in comparison to the module lifetime mean value is calculated.

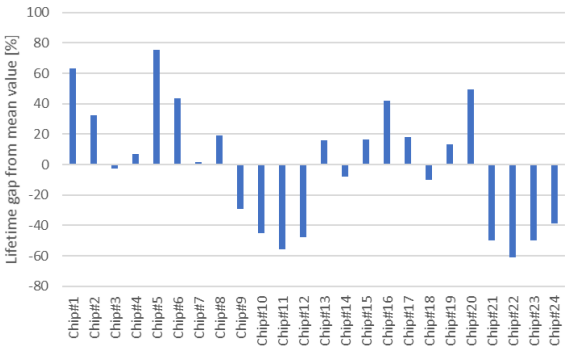


Figure 12 Estimation of lifetime using rainflow counting methodology at chip level.

The following figure illustrates the ΔT counting for the hottest chip vs the single switch mean value.

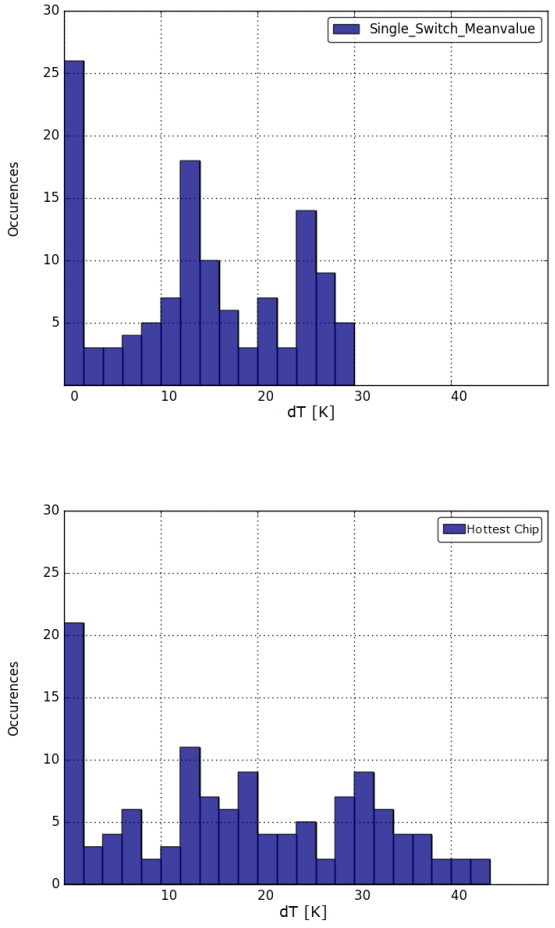


Figure 13 ΔT counting histogram for the most constrained chip of the Single switch studied (bottom) vs module mean value (top).

The same approach has been followed for the New High Power Half-Bridge Module composed of 16 chips.

First, the current distribution at chip level is simulated and determined for the same route profile of the single switch in figure 10.

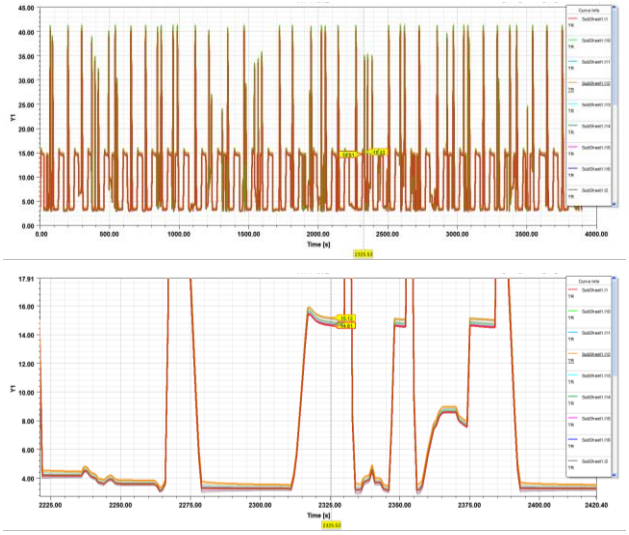


Figure 14 New High Power Half-Bridge current distribution simulation at chip level on a complete route profile.

Based on this current distribution, the figure 15 illustrates the thermal constraint repartition at chip level. A difference lower than 4 K between the coolest and hottest chips is observed.

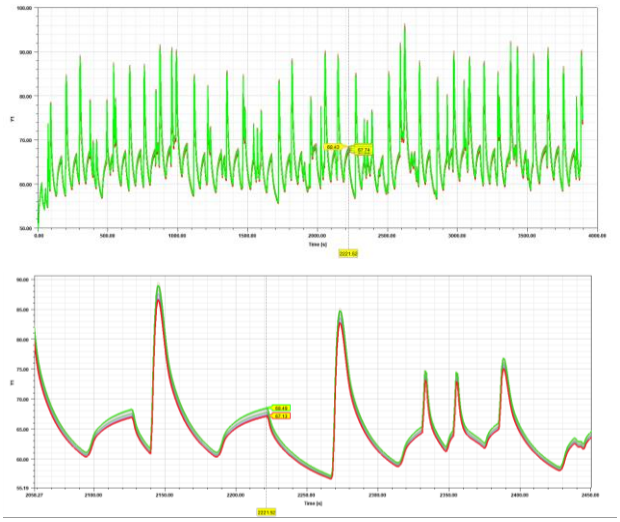


Figure 15 New High Power Half-Bridge chips junction temperature unbalance simulation at chip level on a complete route profile.

Based on this temperature distribution over the complete route profile, the corresponding lifetime is estimated with the same ΔT counting methodology as in figure 12. The histogram on figure 16 represents the lifetime gap from mean value for the 16 chips. Thanks to the construction of the module and to the homogeneous stress distribution described in chapter 2, the repartition of lifetime is significantly improved. A lifetime reduction of 15% is observed for the most constrained chip in comparison to the module mean lifetime.

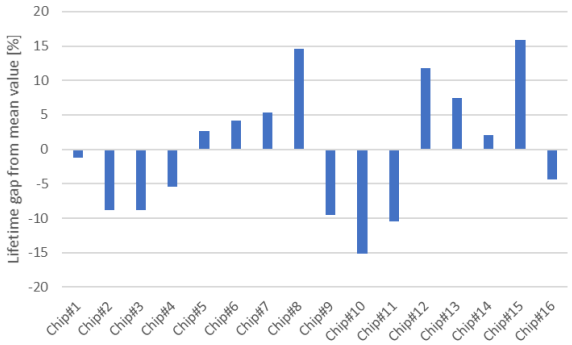


Figure 16 Estimation of lifetime using rainflow counting methodology at chip level.

The figure 17 illustrates the ΔT counting for the hottest chip of the High Power Half-Bridge module.

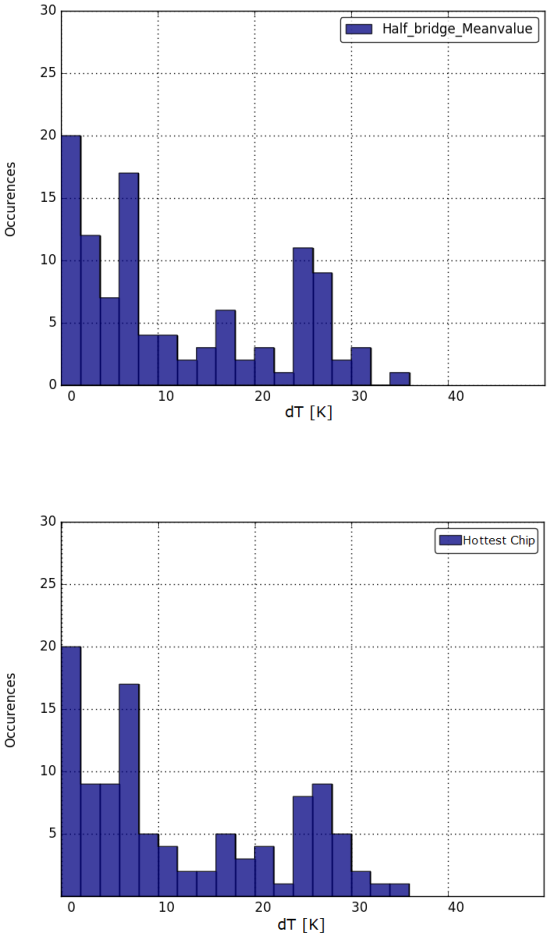


Figure 17 ΔT counting histogram for the most constrained chip of the High Power Half-Bridge studied (bottom) vs module mean value (top).

Summary of comparison of single switch and New Half bridge configuration in terms of current distribution, temperature difference between chips (difference between hottest and coolest chip) is given in figure 18.

	Current distribution	Temperature difference between chips	Lifetime reduction on the most constrained chip
Single switch	**20 %**	**10 K**	**-60%**
New Half bridge module	**3 %**	**<4 K**	**-15%**

Figure 18 Synthesis of the comparison between single switch and High power half-bridge module.

5 Conclusion

In addition to improvement of overall converter performances in terms of power density and compacity, introduction of New High Power Half Bridge Modules in railway converters also improve stress distribution in current and temperature.

New High Power Half-Bridge Modules allow more symmetrical converter design resulting in very good current distribution between chips (from 20 % to 3%).

Thanks to advanced multi-domain simulations based on Reduced Order Model (ROM) technique, it was possible to quantify impact of temperature distribution (reduced by half compared to state-of-the-art modules) on lifetime estimation on a real metro mission profile.

Multi-domain simulations based on Reduced Order Model make possible simulation with the level of accuracy reached by 3D-models with very short computational time, it is very promising to further optimize converter design.

6 Literature

[1] *New generation power semiconductor - Common specification of new generation power semiconductor for railway traction applications* R2R-T1.1-T-BTS042-01 – Roll2Rail – Contract H2020-636032 - November 2016

[2] *Paralleling Reference Setup* – Shift2Rail https://projects.shift2rail.org/download.aspx?id=bec19d25-a8c1-437c-8352-574a4d68f427

[3] U. Scheuermann, *Packaging and Reliability of Power Modules – Principles, Achievements and Future Challenges* – PCIM Europe 2015 – Nüremberg, Germany

[4] M. Piton, B. Chauchat, J.F. Serviere, *Implementation of Direct Chip Junction Temperature Measurement in High Power IGBT Module in Operation - Railway Traction Converter* ESREF 2018, 1892, pp.xxx.

[5] E. Batista and all, *Alstom multi-physics modelling methodology for railway electrical system*, UGM ANSYS conference , Nov. 2011

[6] ASTM E1049-85(2017), *Standard Practices for Cycle Counting in Fatigue Analysis*, ASTM International, West Conshohocken, PA, 2017, www.astm.org

[7] Bernd Laska and Jan Weigel, *New Traction Converter with low inductive High-Voltage Half Bridge IGBT Module* , PCIM 2018

[8] Reinhold Bayerer, *Power Circuit Design for Clean Switching*, CIPS2010

[9] Reinhold Bayerer, *Power Circuit for Clean Switching and low losses*, ECPE tutorial, 2019

[10] Mohsen Akbari and all, *Non-uniform Temperature Distribution Implications on Thermal Analysis Accuracy of Si IGBTs and SiC MOSFETs*, Therminic 2018, Stockholm

Acknowledgement

The authors want to thank Damien Tisné-Grimaud and Yann Daguin from Alstom Traction Design department for their contribution in the thermal 3D modeling and the thermal ROM creation part of this work.

The work was partially supported by the Shift2Rail JU under grant agreement 730668.